Patent

Attorney Docket No. 017750-416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Mail Stop AF**

In re Patent Application of
Grêgory S. Andre
Application No.: 09/955,961
Filing Date: September 20, 2001
Title: TWO LEVEL MULTI-TIER SYSTEM BUS

Group Art Unit: 2112
Examiner: Christopher Lee
Confirmation No.: 1901

## AMENDMENT/REPLY TRANSMITTAL LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed is a reply for the above-identified patent application.

☐ A Petition for Extension of Time is also enclosed.

☐ Terminal Disclaimer(s) and the ☐ $65.00 (2814) ☐ $130.00 (1814) fee per Disclaimer due under 37 C.F.R. § 1.20(d) are also enclosed.

☐ Also enclosed is/are _____

☐ Small entity status is hereby claimed.

☐ Applicant(s) requests continued examination under 37 C.F.R. § 1.114 and enclose the ☐ $395.00 (2801) ☐ $790.00 (1801) fee due under 37 C.F.R. § 1.17(e).

☐ Applicant(s) requests that any previously unentered after final amendments not be entered. Continued examination is requested based on the enclosed documents identified above.

☐ Applicant(s) previously submitted _____

on _____,
for which continued examination is requested.

☐ Applicant(s) requests suspension of action by the Office until at least _____, which does not exceed three months from the filing of this RCE, in accordance with 37 C.F.R. § 1.103(c). The required fee under 37 C.F.R. § 1.17(i) is enclosed.

☐ A Request for Entry and Consideration of Submission under 37 C.F.R. § 1.129(a) (1809/2809) is also enclosed.

☒ No additional claim fee is required.

☐ An additional claim fee is required, and is calculated as shown below.

| AMENDED CLAIMS | | | | | |
|---|---|---|---|---|---|
| | **No. of Claims** | **Highest No. of Claims Previously Paid For** | **Extra Claims** | **Rate** | **Additional Fee** |
| Total Claims | 31 | MINUS 31 = | 0 | x $50.00 (1202) = | $ 0.00 |
| Independent Claims | 2 | MINUS 3 = | 0 | x $200.00 (1201) = | $ 0.00 |
| If Amendment adds multiple dependent claims, add $360.00 (1203) | | | | | |
| Total Claim Amendment Fee | | | | | $ 0.00 |
| ☐ Small Entity Status claimed - subtract 50% of Total Claim Amendment Fee | | | | | $ 0.00 |
| **TOTAL ADDITIONAL CLAIM FEE DUE FOR THIS AMENDMENT** | | | | | **$ 0.00** |

☐ A check in the amount of _____ is enclosed for the fee due.

☐ Charge _____ to Deposit Account No. 02-4800.

☐ Charge _____ to credit card. Form PTO-2038 is attached.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, 1.20(d) and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in duplicate.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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Alexandria, Virginia 22313-1404
(703) 836-6620

By _____
John F. Guay
Registration No. 47,248

Date: February 24, 2005

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| In re Patent Application of | |
| Gregory S. Andre | Group Art Unit: 2112 |
| Application No.: 09/955,961 | Examiner: Christopher Lee |
| Filed: September 20, 2001 | Confirmation No.: 1901 |
| For: TWO LEVEL MULTI-TIER SYSTEM BUS | |

## REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated November 24, 2004, Applicant respectfully requests reconsideration and withdrawal of the rejections of the claims.

In Section 3 of the Office Action, claims 1-7, 14-26 and 28-31 were rejected under 35 U.S.C. §103 as being unpatentable over Kimura (Japanese publication no. JP 409022380 A) in view of Yamagami et al. (Japanese publication no. JP 408272756 A) and pages 39-45 and 76-89 of the PCI publication (Shanley et al., PCI System Architecture, Third Edition, Mind Share, Inc., 1995). This rejection is respectfully traversed.

In section 6 of the Action, beginning on page 12, the Examiner states that Applicant's arguments presented on page 10 of the response filed August 19, 2004, were not considered persuasive, for the following reasons:

A. The Action states that one of the features upon which Applicant relied on is his argument was not relevant to the claimed invention. Specifically, the

Examiner asserts the description in the PCI publication of an arbiter that monitors an IRDY# signal is not related to the claimed invention because "Applicant's invention is not dealing with the subject matter 'bus parking', and further, the PCI standard IRDY# signal is not a dependent signal of 'bus parking' ..." (page 13, lines 12-14). However, it is believed that the Examiner misses the point being made in Applicant's remarks. As pointed out in the response, the arbiter of the PCI publication system can operate to determine if the bus is busy before parking the bus on a PCI device by monitoring the IRDY# signal, which the Examiner relies upon in the Action for meeting the recited busy signal. Because claim 1 recites, among other features, that *means for arbitrating access* establishes a clear path to a destination device by checking device busy *signals* to ensure that the destination device is not busy, and the Examiner identifies the arbiter as a means for arbitrating (see page 3, line 15), the remarks concerning bus parking were directed to pointing out how the arbiter utilizes the IRDY# signal, and why the IRDY# signal of the PCI publication does not teach or suggest a busy signal as claimed.

With respect to a bus arbiter sampling signals *per se*, the cited parts of the PCI publication mention only that the arbiter samples the IRDY# and FRAME# to determine whether the bus is idle before parking the bus on a master, and sampling bus requests REQ# from PCI devices, from which it determines which device to issue a grant GNT# to use the bus. (See, sequence 1 on page 85, sequence 3 on page 86, and lines 1-4 of sequence 12 on page 87.)

With respect to bus parking, when the bus arbiter samples a signal on the IRDY# line, it knows only that a device currently using the bus is performing a transaction of some kind with a target device. This IRDY# signal sampled by the PCI

system arbiter also would only pertain to only *one master device* (i.e., the one currently using the bus).

With regard to sampling a bus request REQ#, the arbiter processes such requests, determines which order is to be taken by the requesting devices, and grants the next determined device the bus. (See, sequence number 3 on page 86.) However, the arbiter does not appear to know, or even care whether any *destination device* is busy because it is up to the granted bus master (initiator device) to determine an idle bus condition before the master device can begin a transaction. The granted bus master does this by monitoring the FRAME# and IRDY# signal lines until it detects that both are deasserted. Because the signals sampled by the PCI system arbiter do not relate to *busy signals* as claimed, they cannot teach or suggest the claimed combination of features including means for arbitrating access to at least a first portion of the system bus among at least two processors to transfer information over the first portion, where the means for arbitrating establishes a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy.

B. In response to Applicant's argument that the description of sequence 6 on page 86 of the PCI publication, which describes sampling IRDY# determine whether target data is *present on the bus,* does not imply, teach or suggest that the signals TRDY# and IRDY# are checked *by an arbiter to ensure that a destination device is not busy* to establish a clear path to the destination device, the Examiner makes the following statements:

> [O]n page 86 at Step 6 states IRDY# is asserted to indicate to the target that the data is present on the bus, and IRDY# and TRDY# are sampled asserted and the first data transfer takes place, which inherently implies that the

> claimed limitations "establishing a clear path to a device (i.e., PCI bus from initiator device to target device) by checking busy signals (i.e., TRDY#) to ensure that said destination device is not busy (i.e., target device is ready). (Page 13, lines 14-19.)

However, the initiator (master) device of the PCI publication system determines whether a particular destination device (i.e., target device) is ready and not the bus arbiter of this system. Put another way, the IRDY# and TRDY# signal "sampling" described in sequence 6 relied upon by the Examiner is not performed by the arbiter, but by a transaction initiator (bus master) and a target device. More particularly, the IRDY# and TRDY# signals are respectively asserted by the bus master and the target device only *after* the master has been granted access to the bus (i.e., after GNT# is sampled asserted by the master device) *and* after FRAME# has been asserted by the master to address the target device. (See, e.g., clock periods 2-3 of Figure 6-3). Before FRAME# can be asserted by the master, however, a *master* waiting to perform a transfer must first check whether the bus is idle. (See, page 82, lines 6-7of the section entitled "Hidden Bus Arbitration.") This is accomplished by the *master device* sampling signals on the FRAME# and IRDY# lines (e.g., see sequence 2 on page 86). If the FRAME# and IRDY# signals are sampled as deasserted by the bus master and target devices, the bus is determined to be idle and the transaction proceeds. (See, Table 6-1 on page 85.) Hence, the arbiter does not sample "busy signals" as alleged by the Examiner. Furthermore, the cited parts of the PCI publication are silent with respect to the arbiter *ever* sampling the TRDY# line.

Hence, the IRDY# and TRDY# signals described in the cited parts of the PCI publication do not teach or suggest the claimed feature of "means for arbitrating establishing a clear path to a destination device by checking busy *signals* to ensure

the destination device is not busy." Nor is this feature inherently taught in the PCI publication. For instance, there may not be a clear path to a target device when a master device next granted access to the bus in the PCI system attempts to perform a transaction. Indeed, that is why the bus master must monitor the target TRDY# signal and wait for when the target is ready to receive or transmit data.

By contrast, the apparatus and method of the present application provide advantageous features over the known PCI bus protocol cited in the Office Action. For example, as described in paragraph 0052 of Applicant's specification, checking receiver busy signals of the devices on the system bus during arbitration allows verification that the device to which a processor wishes to transmit is not busy. The well known PCI bus protocol, by contrast, transmits without checking to see if a device is busy, and if a device is busy, continues to abort and retry data packet transmissions, which can overload a system bus and cause critical failures in computing systems.

For all these reasons, it is respectfully submitted that the PCI publication fails to remedy the acknowledged deficiencies of Kimura, the Yamagami et al. documents. Therefore, the rejection fails to establish a *prima facie* case of obviousness with respect to independent claim 1. Independent claim 17 recites similar distinctions with respect to a method of managing flow of information among processors and is therefore also considered allowable.

It is respectfully submitted that the Sand et al. and MacDonald et al. patents likewise do not teach or suggest every feature recited in the combinations of features set forth in independent claims 1 and 17. Hence, no combination of the Kimura, Yamagami et al., the PCI publication, and the Sand et al. and McDonald et al.

documents would have taught or suggested what is set forth in the independent claims.

The remaining claims 2-16 and 18-31 depend from one of independent claims 1 and 17 and recite further advantageous features which further distinguish over the documents relied upon by the Examiner. As such, these claims also are considered patentable.

In view of the foregoing, Applicant respectfully request withdrawal of all rejections so that the application can be passed to issuance without further delay.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: February 24, 2005

By: _____
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